Session 30 Overview

Building Blocks for High-Speed Transceivers

Chair: Michael M. Green, *University of California, Irvine, CA*

Associate Chair: Thomas Burger, *ETH Zurich, Zurich, Switzerland*

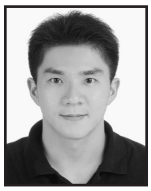
Not long ago, the feasibility of realizing multi-Gb/s transceivers in standard CMOS seemed questionable. However, the rapid decrease in CMOS feature sizes and major advances in analog high-speed design techniques in recent years have made such high-speed performance a reality. Currently, bit rates of 10Gb/s and higher are commonplace even in standard CMOS processes. This session highlights papers exploiting both of these improvements. Two of the papers show extraordinary circuit speeds (70GHz and higher) using a 65nm SOI CMOS process. Five of the papers show very high-speed performance blocks using mature ($\geq$ 0.13µm) CMOS or BiCMOS technologies. Finally, two other papers show how high-performance analog circuit design can allow further integration of systems on a chip.

Two papers demonstrate how a 65nm SOI CMOS process can achieve very high-speed analog circuit blocks. The design presented in Paper 30.3 from MIT and IBM breaks a speed record for a CMOS clock divider that operates up to 100GHz input frequency. Paper 30.2 from IBM, Yale and MIT, describes an LC-VCO that oscillates at a center frequency near 70GHz with a tuning range of over 6GHz. Both papers demonstrate the feasibility of volume production over process variations.

The next three papers demonstrate that innovation in circuit design can still yield considerable performance improvements. Papers 30.1 and 30.6 demonstrate amplifiers using standard CMOS that operate near 40GHz: in Paper 30.1 from National Taiwan U, cascaded gain stages in a 0.18µm CMOS are used to maximize the gain-bandwidth product; in Paper 30.6 from U Waterloo, loss compensation using active negative resistance in a 0.13µm CMOS process allows flattening of the frequency response. Paper 30.4 from National Taiwan U cleverly uses series- and shunt-peaking inductors to achieve a wide-range 40GHz clock divider and low-phase-noise VCO using a 0.18µm CMOS process.

Two papers describe the use of circuit design techniques in BiCMOS to greatly enhance performance of broadband ICs. In Paper 30.8 from TU Denmark, Intel, and IPtronics, an active-load circuit replaces the conventional 50Ω back-termination resistor, allowing nearly 50% decrease in the power dissipation of a laser driver. In Paper 30.9 from TU Vienna, the exponential characteristic of a BJT is used to achieve 112dB dynamic range in a TIA for an optical receiver while maintaining 240MHz bandwidth.

Paper 30.5 from Intel and ASU demonstrates a new on-chip phase-noise measurement technique that achieves -75dBc single-tone sensitivity at a 100kHz offset frequency for carrier frequencies up to 2GHz. Paper 30.7 from TU Munich, Stanford, and Infineon shows that effective ESD protection can co-exist with high-speed I/Os: 2kV protection is achieved on an input pad in a 90nm CMOS process while still exhibiting a bandwidth of over 10GHz.



30.1 40Gb/s High-Gain Distributed Amplifiers with Cascaded Gain Stages in 0.18µm CMOS **1:30 PM**

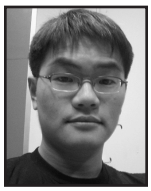
J-C. Chien, National Taiwan University, Taipei, Taiwan

High-gain distributed amplifiers (DA) using cascaded stages as distributed cells are implemented in 0.18µm CMOS technology. Two DAs with 3×3 and 2×4 configurations are demonstrated for 40Gb/s applications. While consuming 250mW from a 2.8V supply, a GBW of up to 394GHz is achieved.

30.2 A 70GHz Manufacturable Complementary LC-VCO with 6.14GHz Tuning Range in 65nm SOI CMOS **2:00 PM**

D. Kim, IBM, Hopewell Junction, NY

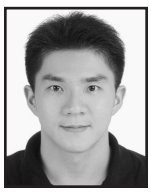
A complementary LC-VCO is integrated in a 65nm SOI process and is statistically characterized on a 300mm wafer. Average center frequency is 67.9GHz and frequency tuning range is 6.14GHz or 9.05%. It achieves a phase noise of -106dBc/Hz at 10MHz offset and consumes 5.37mW from a 1.2V supply. The VCO yield is 94.7% for 70GHz operation.



30.3 Performance Variability of a 90GHz Static CML Frequency Divider in 65nm SOI CMOS **2:15 PM**

D. Lim, Massachusetts Institute of Technology, Cambridge, MA

A static CML divide-by-2 frequency divider is integrated in 65nm SOI CMOS. The maximum operating frequency is 90GHz while dissipating 52.4mW. The self-oscillation frequency is 92GHz with 0.57pJ switching energy. Measurement of self-oscillation frequency at multiple bias conditions enables estimation of the variation in threshold voltage, capacitance, and resistance.



30.4 40GHz Wide-Locking-Range Regenerative Frequency Divider and Low-Phase-Noise Balanced VCO in 0.18µm CMOS **2:30 PM**

J-C. Chien, National Taiwan University, Taipei, Taiwan

A 40GHz wide-locking-range frequency divider and a low-phase-noise VCO are implemented in 0.18µm CMOS technology. The frequency divider demonstrates a locking range of 10.6GHz with 0dBm input power while the VCO exhibits a phase noise of -108.65dBc/Hz at 1MHz offset. Each of the 2 circuits consumes 6mW from a 1V supply.

30.5 A Self-Calibrated On-Chip Phase-Noise-Measurement Circuit with -75dBc Single-Tone Sensitivity at 100kHz Offset **3:15 PM**

W. Khalil, Intel, Chandler, AZ

An on-chip phase-noise-measurement circuit with single-tone measurement sensitivity of -75dBc at 100kHz offset from carrier is presented. The circuit uses a delay-line and mixer frequency discriminator and can operate up to 2GHz input frequency. This module does not rely on a reference clock and, with on-line self calibration, its accuracy is stabilized across gate-delay variations.

30.6 A 10dB 44GHz Loss-Compensated CMOS Distributed Amplifier **3:45 PM**

K. Moez, University of Waterloo, Waterloo, Canada

An 8-stage distributed amplifier (DA) suitable for 40Gb/s optical communication is implemented in a 0.13µm CMOS process. The losses of on-chip transmission lines are compensated by active negative resistors. The DA achieves a flat gain of 10dB from DC to 44GHz with an input and output matching better than -8dB. The core DA and loss compensation circuitry dissipate 44mW and 59mW, respectively.

30.7 A 10GHz Broadband Amplifier with Bootstrapped 2kV ESD Protection **4:00 PM**

W. Soldner, Technical University Munich, Munich, Germany

A phase-corrected bootstrap circuit for active capacitance compensation of a low-C ESD-protection element is discussed. A broadband 2kV-ESD-protected 10GHz amplifier fabricated in a 90nm CMOS process serves as a test vehicle. Inductive peaking compensates for the intrinsic phase shift of the multi-stage bootstrap circuit.

30.8 45% Power Saving in a 0.25µm BiCMOS 10Gb/s 50Ω-Terminated Packaged Active-Load Laser Driver **4:15 PM**

E. Ayranci, Technical University of Denmark, Kgs. Lyngby, Denmark, and Intel Copenhagen, Skovlunde, Denmark

A 0.25µm BiCMOS laser driver based on active loads allows operation at 10Gb/s while drawing 5mA from a 1.8V supply. The design guarantees the correct matching of the driver outputs without the use of physical 50Ω load resistors. This enables a theoretical current consumption reduction of 50% (45% in the actual prototype) compared to the traditional laser-driver design.

30.9 A 240MHz-BW 112dB-DR TIA **4:30 PM**

D. Micusik, Vienna University of Technology, Vienna, Austria

A non-saturating TIA with 20mA input current overdrive and 48nA equivalent rms input noise current is described. The proposed TIA has a linear region for small input currents and a compressing one for high currents, that would otherwise saturate the TIA. The complete chip including the 50Ω driver occupies 1.24mm^2 in 0.35µm SiGe BiCMOS technology.